

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 2

Applicant Number	10/840,015
Filing Date	May 5, 2004
First Named Inventor	Adrian J. Drexler et al.
Art Unit	2634-2816
Examiner Name	Not Yet Assigned T. Lam
Attorney Docket Number	MIC-44
Confirmation Number	9647

U. S. PATENT DOCUMENT

U. S. PUBLISHED DOCUMENT

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
u		2005/0062510 A1	03/24/05	Zarate et al.	

**Examiner
Signature**

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Sheet 2 of 2

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	
<i>TL</i>		Saeki et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, pp. 1656-1668, (1996).
<i>TL</i>		Shim et al., "An Analog Synchronous Mirror Delay for High-Speed DRAM Application," IEEE Journal of Solid-State Circuits, Vol. 34 No. 4, pp. 484-493, (1999).
<i>TL</i>		Kim et al., "A Low-Jitter Mixed-Mode DLL for High-Speed DRAM Applications," IEEE Journal of Solid-State Circuits, Vol. 35 No. 10, pp. 1430-1436, (2000).

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11/3/05

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Examiner Name	Tuan Thieu Lam
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		Number-Kind Code ² (if known)			
JK		2002/190766	12/19/2002	Waldrop	
JK		2003/081472	05/01/2003	Lin	
JK		2004/044918	03/04/2004	Dermott et al.	
JK		2004/057331	03/25/2004	Graaff	

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